[Total No. of Questions - 9] [Total No. of Printed Pages - 3] (2125)

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# B. Tech 4th Semester Examination Electronic Logic Circuit Design (OS) EC-4003

Time: 3 Hours Max. Marks: 100

The candidates shall limit their answers precisely within the answerbook (40 pages) issued to them and no supplementary/continuation sheet will be issued.

**Note:** Attempt five questions in all, selecting one question each from section A, B, C & D. Section-E is compulsory.

### **SECTION - A**

- 1. (a) Convert S-R flip-flop to T flip- flop.
  - (b) Design 3-bit binary up-down counter circuit using T flipflop. (12)
- Draw a two input, two output synchronous sequential circuit which produces an output z=1 whenever any of the following input sequences occur: 1100, 1010, or 1001. The circuit resets to its initial state after a 1 output has been generated. Use J-K flip-flop in your realization. (20)

#### **SECTION - B**

3. For each of the machines shown in table 1 and 2, find a minimum state reduced machine containing the original one.

	Table	e 1	
PS	NS,Z		
	I <sub>1</sub>	I <sub>2</sub>	l <sub>3</sub>
Α	C,0	E,1	-
В	C,0	E,-	-
С	В,-	C,0	Α,-
D	B,0	С,-	E,-
Е	9	E,0	Α,-

	Table 2		
PS	NS,z		
	x=0	x=1	
Α	B,1	H,1	
В	F,1	D,1	
С	D,0	E,1	
D	C,0	F,1	
Е	D,1	C,1	
F	C,1	C,1	
G	C,1	D,1	
Н	C.0	A.1	

[P.T.O.]

(8)

(20)

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4. What is meant by decomposition? Compare the various decomposition techniques in detail. (20)

#### SECTION - C

- 5. Give a minimum row, reduced flow table description of a two input (x<sub>1</sub>, x<sub>2</sub>), one output (z) sequential circuit which operates in the following manner: z=1 if and only if x<sub>1</sub>=x<sub>2</sub>=1 and the next to last input variable change was a change of x<sub>i</sub>. Assume that the circuit is initially in the state x<sub>1</sub>=x<sub>2</sub>=0. (20)
- Design a asynchronous sequential circuit with two inputs, x<sub>1</sub> and x<sub>2</sub>, and two output z<sub>1</sub> and z<sub>2</sub>, is to be designed so that z<sub>i</sub> (for i=1,2) takes on the value 1 if and only if x<sub>i</sub> was the input that changed last. (20)

#### SECTION - D

7. (a) Design a hazard free combinational circuit for the function given below:

$$F(A,B,C,D) = \Sigma m(0,1,2,3,4,7,8,9,12,13)$$
(10)

(b) Explain, Essential Hazards in Asynchronous sequential circuits. (8)

## **SECTION - E**

- (a) Write different steps for the synthesis of Asynchronous sequential circuits.
  - (b) Differentiate between synchronous and asynchronous sequential circuits.
  - (c) What are fundamental mode circuits?

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- (d) Prove that the equivalence partition is unique.
- (e) Why races are introduced in asynchronous sequential circuits?
- (f) What is meant by propagation delay?
- (g) Why state assignment is important in asynchronous sequential circuits?
- (h) Draw the circuit of parallel in parallel output register using j-k flip-flops?
- (i) What do you mean by static-1 hazard in digital circuits?
- (j) Two states are k-distinguishable. What does it mean? (2×10=20)